WHAT IS CLAIMED IS:

1. An at least two-bit equalization system to adjust an amplitude of an input signal in a channel for a channel amplitude frequency response, comprising:

a decision subsystem to decide when the input signal is to be adjusted, and to produce a delayed input signal and at least two output signals utilized to assist in adjusting the input signal;

an equalization step selection subsystem to select equalization step adjustment sizes to adapt to transmit media variations; and

an equalization subsystem to receive the delayed input signal, the at least two output signals from the decision subsystem, and the equalization step adjustment sizes from the equalization step selection subsystem, to apply the equalization step adjustment sizes to the at least two output signals, and to produce an equalized output signal compensated for the channel amplitude frequency response.

2. The equalization system of claim 1, wherein n is a number of bits equalized in the equalization system and m is a number of output signals generated by the decision subsystem, the equalization system having:

n greater than two; and

m equal to n.

3. A transmitting device to send an input signal on a channel, comprising:

an equalization system to perform at least a two-bit equalization, including

a decision subsystem to decide when the input signal is adjusted, and to

produce a delayed input signal and at least two output signals to assist in adjusting the input signal, and

an equalization step selection subsystem to select equalization step adjustment sizes to adapt to transmit media variations; and

an equalization subsystem to receive the delayed input signal, the at least two output signals from the decision subsystem, and the equalization step adjustment sizes from the equalization step selection subsystem, to apply the equalization step adjustment sizes to the at least two output signals, and to produce an equalized output signal compensated for the channel amplitude frequency response.

a transmitter to send the equalized output signal to the channel.

4. The transmitting device according to claim 3, wherein n is a number of bits equalized in the equalization system and m is a number of output signals generated by the decision subsystem, the transmitting device having:

n greater than 2; and

m equal to n.

5. A transmitting device according to claim 3, wherein the channel is a printed circuit board trace.

6. A transmitting device according to claim 3, wherein the channel is a copper wire channel.

7. A transmitting device according to claim 3, wherein the channel is an optical fiber channel.

8. A method for at least two-bit equalization of an input signal to compensate for a channel frequency response, comprising:

generating a delayed input signal;

generating at least two intermediate output signals to identify if and when adjustments need to be made to the input signal;

converting the delayed input signal and the at least two intermediate output signals to a differential delayed input signal and at least two differential intermediate output signals;

selecting an equalization step size for each of the at least two intermediate output signals based on the channel frequency response;

dividing a tail current into at least three weighted current segments based on the equalization step size;

inputting the differential delayed input signal, the at least two differential intermediate output signals, and the at least three weighted current segments into at least three differential pairs that output at least three output currents; and

combining the at least three output currents to form an equalized output signal.

9. The method of claim 8, wherein the weight of the weighted current segments is determined, by default set or by user, by a plurality of control bits in a control subsystem.

10. The method of claim 9, wherein the number of control bits is six.

11. A two-bit equalization system to output an equalized signal compensated for a channel frequency response, comprising:

a decision subsystem to decide when an input signal is adjusted and to output a delayed input signal and two output signals, the decision subsystem having

a delay module to align the input signal with the two output signals,

an exclusive-or (XOR) circuit, an inverted exclusive-or (XNOR) circuit, and a delay module to output a first output signal,

a XOR circuit, an or circuit, and a XNOR circuit to output a second output signal; and

an equalization subsystem to output the equalized signal compensated for a channel frequency response having

a tail current switch to direct a tail current,

a plurality of current control bits to partition the tail current into three branches with an amount of each current predetermined by selected control bits, and

three differential pairs to accept as input the partitioned tail current branches, the delayed input signal, the first output signal, and the second output signal from the decision subsystem, and to output three currents that are combined to form the equalized signal.

12. The two-bit equalization system of claim 11, wherein the number of current control bits is six.

13. A transmitting device to send an input signal on a channel, comprising:

an equalization system to perform at least a two-bit equalization, including:

a decision subsystem to decide when an input signal is adjusted and to output a delayed input signal and at least two output signals, the decision subsystem having:

a delay module to align the input signal with the two output signals,

an exclusive-or (XOR) circuit, an inverted exclusive-or (XNOR) circuit, and a delay module to output a first output signal,

a XOR circuit, an or circuit, and a XNOR circuit to output a second output signal; and

an equalization subsystem to produce an equalized output signal compensated for a channel frequency response having:

a tail current switch to direct a tail current,

a plurality of current control bits to partition the tail current into three branches with an amount of each current predetermined by selected control bits, and

at least three differential pairs to accept as input the partitioned tail current branches and the delayed input signal, the first output signal, and the second output signal from the decision subsystem, and to output three currents that are combined to form the equalized output signal; and

a transmitter to send the equalized output signal as the input signal to the channel.

14. A transmitting device according to claim 13, wherein the channel is a printed circuit board trace.

15. A transmitting device according to claim 13, wherein the channel is a copper wire channel.

16. A transmitting device according to claim 13, wherein the channel is an optical fiber channel.

17. A machine readable storage medium, comprising:

machine-readable program code, stored on the machine readable storage medium, the machine-readable program code having instructions to

generate a delayed input signal;

generate at least two intermediate output signals to identify if and when adjustments need to be made to the input signal;

convert the delayed input signal and the at least two intermediate output signals to a differential delayed input signal and at least two differential intermediate output signals;

selecting an equalization step size for each of the at least two intermediate output signals based on the channel frequency response;

dividing a tail current into at least three weighted current segments based on the equalization step size;

input the differential delayed input signal, the at least two differential intermediate output signals, and the at least three weighted current segments into at least three differential pairs that output at least three output currents; and

combine the at least three output currents to form an equalized output signal.

18. The machine readable storage medium of claim 17, wherein the tail current is divided into three weighted current segments by a plurality of selected control bits.

19. The machine readable storage medium of claim 18, wherein the tail current is divided into three weighted current segments by six control bits.